SYSTEM FOR CONTROLLING EXTERNAL MODELS USED FOR VERIFICATION OF SYSTEM ON A CHIP (SOC) INTERFACES

ABSTRACT

A method and structure for a verification test bench system for testing an interface of a system-on-a-chip (SOC) that includes a verification interface model connected to the SOC interface and a test bench external bus interface unit (EBIU) connected to the verification interface model. The test bench EBIU is connected to a SOC EBIU within the SOC. The test bench EBIU and the SOC EBIU are mastered by the same processor in the SOC, such that the SOC interface and the verification interface model are programmed by the same test case running in the SOC.